a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film interposed therebetween, said second semiconductor layer comprising a second channel formation region and second source and drain regions being in contact with said second channel formation region,

wherein said second gate electrode partially overlaps said second source and drain regions, and

wherein a wiring is connected to said at least one of said second source and drain regions.

REMARKS

The following comments are in response to the Examiner's objections and rejection in the Final Rejection.

I. Informalities In The Claims

In the Final Rejection, the Examiner has a number of objections to informalities in the claims. Applicants have amended Claims 1, 6, 11, 14, and 19 to correct these informalities. It is respectfully submitted that as amended, the claims are in an allowable condition.

II. Prior Art Rejections

The Examiner also has the following rejections under 35 USC §103:

a. Claims 11-13 as being unpatentable over Miyasaka et al.;

b. Claims 1-4 and 6-9 as being unpatentable over Miyasaka et al. in view of Kondo;

c. Claims 14-17 and 19-22 as being unpatentable over Miyasaka et al. in view of Kondo, further in view of Johnson; and

d. Claims 24-26 as being unpatentable over Miyasaka et al. in view of Johnson.

The Examiner, however, stated that Claims 5, 10, 18 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Therefore, in order to advance the prosecution of this case, Applicants have amended independent Claims 1, 6, 14 and 19 to add the limitation ("wherein said semiconductor layer of said p-channel TFT has no LDD regions") from these dependent claims (as they all depend directly from an independent claim). Accordingly, each of these amended independent claims and the claims dependent thereon are allowable over the cited references.

Applicants have also amended independent Claims 11 and 24 to recite that said p-channel TFT includes a second semiconductor layer, "said second semiconductor layer comprising a second channel formation region and second source and drain regions being in contact with said second channel formation region." As a result, the semiconductor layer of the p-channel TFT has no LDD regions. Therefore, for substantially the same reasons dependent claims 5, 10, 18 and 23 were deemed allowable by the Examiner, these independent claims and the claims dependent thereon are also allowable over the cited references.

Accordingly, for the above-stated reasons, it is respectfully submitted that the claims are patentable, and the rejections under §103 should be withdrawn.

III. Entry of Amendment

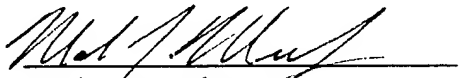
In this Amendment, Applicants are correcting informalities and incorporating in the independent claims, features from dependent claims that were already present, examined and allowed by the Examiner. Accordingly, it is not believed that any further search or examination is necessary in response to this amendment. Therefore, since the Amendment is merely placing the application in a condition for allowance, it is respectfully requested that the amendment be entered, and the application passed to allowance.

If any fee is due for this amendment, please charge our deposition account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Dated: June 10, 2002



Mark J. Murphy
Registration No. 34,225

COOK, ALEX, McFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
200 West Adams Street, Suite 2850
Chicago, Illinois 60606
(312) 236-8500

Marked-up copy of the claims as amended:

IN THE CLAIMS:

Please amend the claims as follows:

1. **(Fourth Amendment)** A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions[.],

wherein said semiconductor layer of said p-channel TFT has no LDD regions.

Cancel Claim 5.

6. **(Thrice Amended)** A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein the portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT does not overlap said [second] first source and drain regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions[.],

wherein said semiconductor layer of said p-channel TFT has no LDD regions.

Cancel Claim 10.

11. **(Thrice Amended)** A ferroelectric liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region,

and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions;

wherein said first gate electrode partially overlaps said [first impurity region] pair of LDD regions, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film interposed therebetween, said second semiconductor layer comprising a second channel formation region and [a third impurity region] second source and drain regions being in contact with said second channel formation region,

wherein second gate electrode partially overlaps said [third impurity region] second source and drain regions, and

wherein a wiring is connected to [said third impurity region] at least one of said second source and drain regions.

14. **(Thrice Amended)** A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT is partially overlaps said second source and drain regions[.],

wherein said semiconductor layer of said p-channel TFT has no LDD regions.

Cancel Claim 18.

19. **(Thrice Amended)** A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein the portion which said second conductive layer is in contact with said gate insulating film in said n-channel [region] TFT does not overlap said first source and drain regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions[.],

wherein said semiconductor layer of said p-channel TFT has no LDD regions.

Cancel Claim 23.

24. **(Thrice Amended)** A goggle type display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions;

wherein said first gate electrode partially overlaps said [first impurity region] pair of LDD regions, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and [a third impurity region] second source and drain regions being in contact with said second channel formation region,

wherein said second gate electrode partially overlaps said [third impurity region] second source and drain regions, and

wherein a wiring is connected to said [third impurity region] at least one of said second source and drain regions.